UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,328	12/14/2001	David M. Fried	BUR920010171	8627

23389 7590 12/18/2003

SCULLY SCOTT MURPHY & PRESSER, PC
400 GARDEN CITY PLAZA
GARDEN CITY, NY 11530

EXAMINER	
PERALTA, GINETTE	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 12/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	09/683,328	FRIED ET AL.	
	Examin r	Art Unit	
	Ginette Peralta	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,14-18,20-22 and 24-28* is/are pending in the application.

4a) Of the above claim(s) *1-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12,14-18,20-22,24-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claims 12, 20-22, and 24-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Enders et al. (U. S. Pat. 6,503,784 B1).

Regarding claim 12, Enders et al. discloses in Figs. 2S and 5C an asymmetric field effect transistor that comprises a patterned stack including at least a vertical semiconductor body 54a having sidewalls 52 located on an upper surface non-recessed surface of an insulator that is located on a substrate (col. 1, ll. 45-49); a gate dielectric 52 located on the sidewalls of the vertical semiconductor body; a p-type gate portion 56p located on one side of the vertical semiconductor body and an n-type gate portion 56n located on an opposing side of the vertical semiconductor body54 a, the gate portions located on the upper surface of the substrate and are separated from the vertical semiconductor body 54a by the gate dielectric, and an interconnect located at least over

the p-type gate portion and the n-type gate portion and a planarizing structure (110 and metal 1) above the interconnect 1.

Regarding claim 20, Enders et al. discloses the semiconductor body having a hard mask 57 present on an upper surface.

Regarding claim 21, Enders et al. discloses the hard mask comprising an oxide (col. 5, ll. 57-60).

Regarding claim 22, Enders et al. discloses that the n-type gate portion is comprised of N-doped polysilicon and the p-type gate portion is comprised of P-type polysilicon (col. 7, ll. 8-51, col. 8, ll. 1-16).

Regarding claim 24, Enders et al. discloses in Fig. 2O that the substrate comprises an upper insulating portion 80 and a lower semiconducting portion 14 and in col. 1, ll. 45-49 it is disclosed that the an insulating layer extends horizontally beneath the pair of transistors.

Regarding claim 25, Enders et al. discloses in Fig. 5C that part of the planarizing material is METAL 1.

Regarding claim 26, Enders et al. discloses source/drain regions in areas adjacent to the vertical semiconductor body (3D, 6D, 6S, etc.).

Regarding claim 27, Enders et al. discloses that the source/drain regions are doped so as to have either donor or acceptor impurities.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 14-18, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Enders et al. in view of Lou et al. (U. S. Pat. 5,872,045).

Regarding claims 14, 15, and 18, Enders et al. discloses that the p-type gate portion and the n-type gate portion are composed of a polysilicon containing material. Enders et al. further discloses that the planarizing structure comprises silicon oxide.

Enders et al. discloses the claimed invention with the exception of using undoped polysilicon for the planarizing structure.

Lou et al. discloses a method for making an improved global planarization surface that includes the use of silicon oxide or undoped polysilicon for the planarized surface, wherein the polysilicon is used for the disclosed intended purpose of resulting in an improved global planarity which also improves the polysilicon dishing in the edges of the substrate.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use either silicon oxide or undoped polysilicon as Lou et al. teaches in the invention of Enders et al. for the disclosed intended purpose of obtaining

a structure having an improved global planarity which also improves the polysilicon dishing in the edges of the substrate.

Regarding claims 16 and 17, Enders et al. disclose the use of various materials for the conductive layers including the use of titanium, titanium nitride, titanium silicide and tungsten among others to form contacts and interconnections. It is an inherent property of these materials to be highly resistant to dopant diffusion. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use any of the above recited metals as used by Enders et al. in the contacts and metal layers as the interconnect material.

Regarding claim 28, Enders et al. discloses in Figs. 2S and 5C a field effect transistor that comprises a p-type gate portion 56p and an n-type gate portion 56n on a vertical single crystal Si semiconductor body 54a; the p-type and n-type gate portions are composed of polysilicon; a metal interconnect 1 between the p-type gate portion 56p and the n-type gate portion 56n; and a planarizing structure (110 and metal 1) above the interconnect 1; Enders et al. further discloses in Figs. 2S and 5C a field effect transistor that comprises a patterned stack including at least a vertical semiconductor body 54a having sidewalls 52 located on an upper surface of a substrate; a gate dielectric 52 located on the sidewalls of the vertical semiconductor body; a p-type gate portion 56p located on one side of the vertical semiconductor body and an n-type gate portion 56n located on an opposing side of the vertical semiconductor body54 a, the gate portions located on the upper surface of the substrate and are separated from the

vertical semiconductor body 54a by the gate dielectric, and an interconnect located at least over the p-type gate portion and the n-type gate portion and a planarizing structure (110 and metal 1) above the interconnect 1.

Response to Arguments

5. Applicant's arguments filed 5/2/03 have been fully considered but they are not persuasive.

With regards to applicant's arguments directed to the newly amended claims, the newly added features are addressed above in the rejections.

With regards to applicant's argument that Enders et al. do not disclose an asymmetric FET which includes, among other features, a patterned stack including at least a vertical semiconductor body having sidewalls located on an upper non-recessed surface of an insulator of substrate, with regards to this, Enders et al. teaches that in accordance with their invention an insulating layer extends horizontally beneath the surface of the semiconductor body such insulating layer being disposed beneath the pair of transistors, with regards to applicant's argument that in Enders et al. the transistors are located in trenches below an upper surface of the semiconductor body, it is noted that although initially the transistors are formed in trenches below the upper surface of the semiconductor body, in the final structure, the surface of the semiconductor body has been reduced to below the transistors, furthermore as shown in fig. 5C, an insulating layer is formed on the surface of the semiconductor body, and

the transistors are beneath the insulating layer and the surface of the semiconductor body.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (703) 305-7722. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

GP

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800